

GA-970A-D3

Revision : 1.1

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24	ALC889R CODEC
25	AUDIO JACK

[illegible]

GIGABYTE™			
Title			
COVER SHEET			
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Custom	GA-970A-D3	1.1	
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Model Name:GA-970A-D3

Component value change history

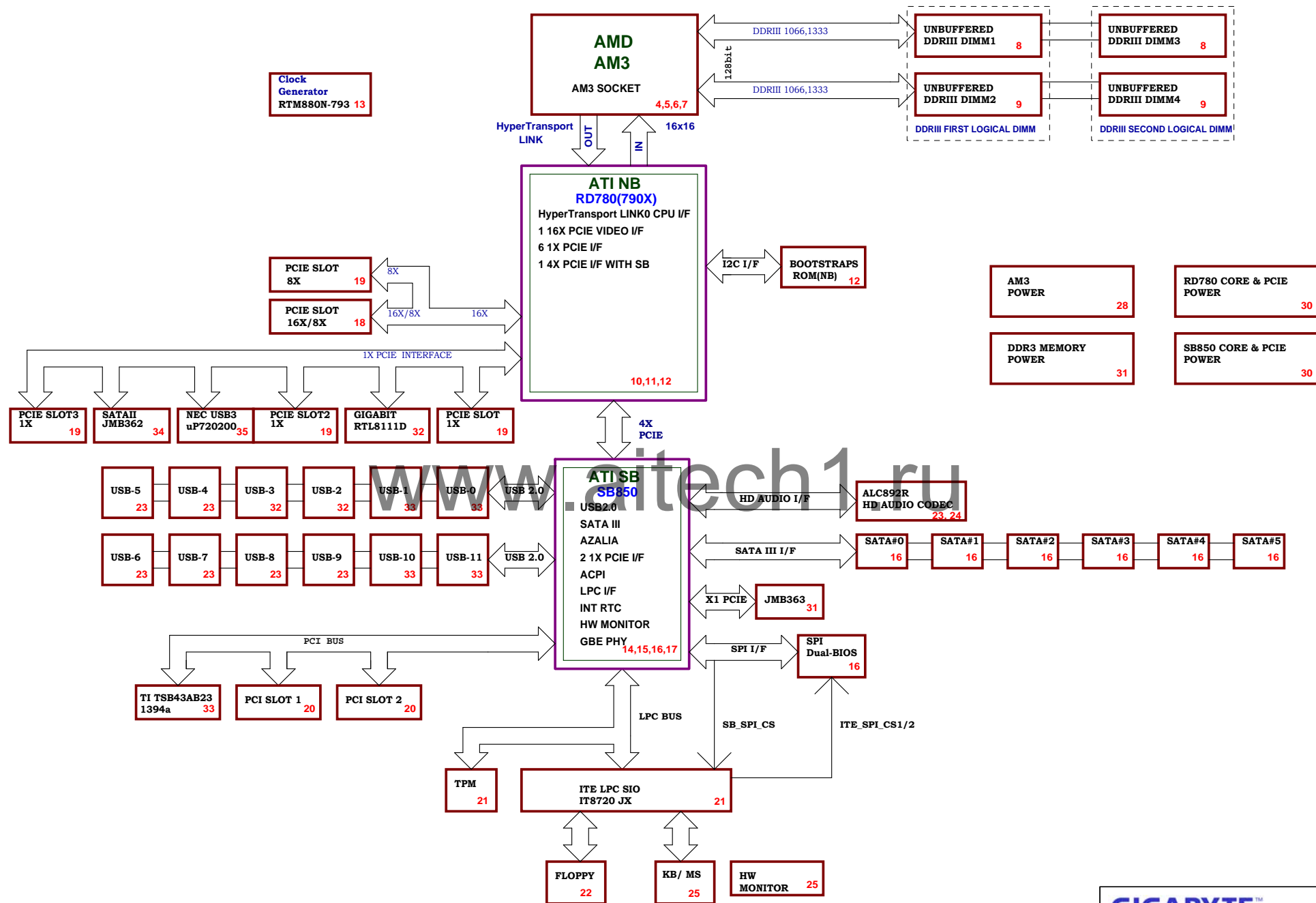
Version: 1.1A

P-Code: U98094-0

[illegible]

Circuit or PCB layout change for next version

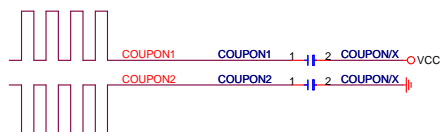
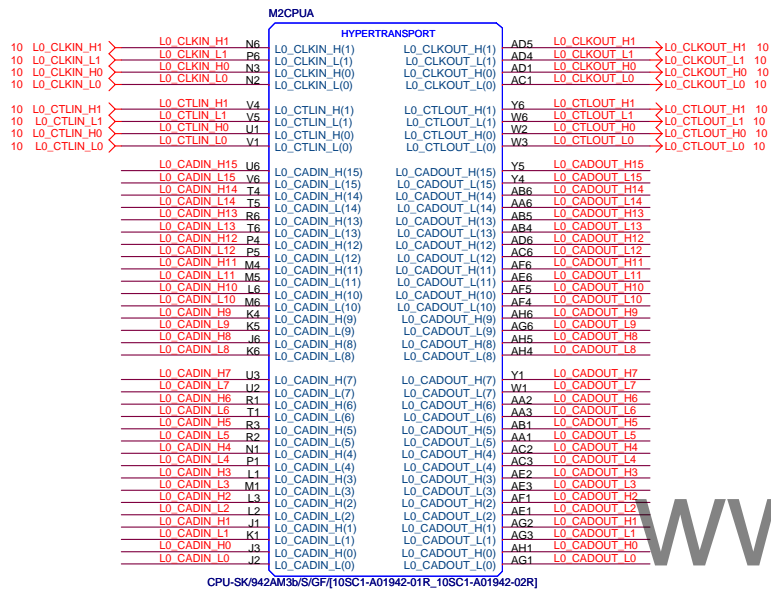
[illegible]



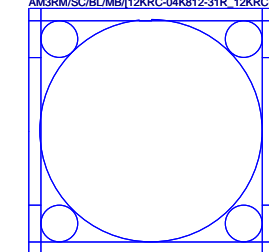
L0_CADIN_L[0..15] <L0_CADIN_L[0..15] 10
L0_CADIN_H[0..15] <L0_CADIN_H[0..15] 10
L0_CADOUT_L[0..15] <L0_CADOUT_L[0..15] 10
L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] 10

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
VLDT_B = HT12B



M2CPU
AM3RM/SC/BL/MB[12KRC-04K812-31R_12KRC-04K812-32R]



GIGABYTE™			
Title			
CPU HYPER TRANSPORT			
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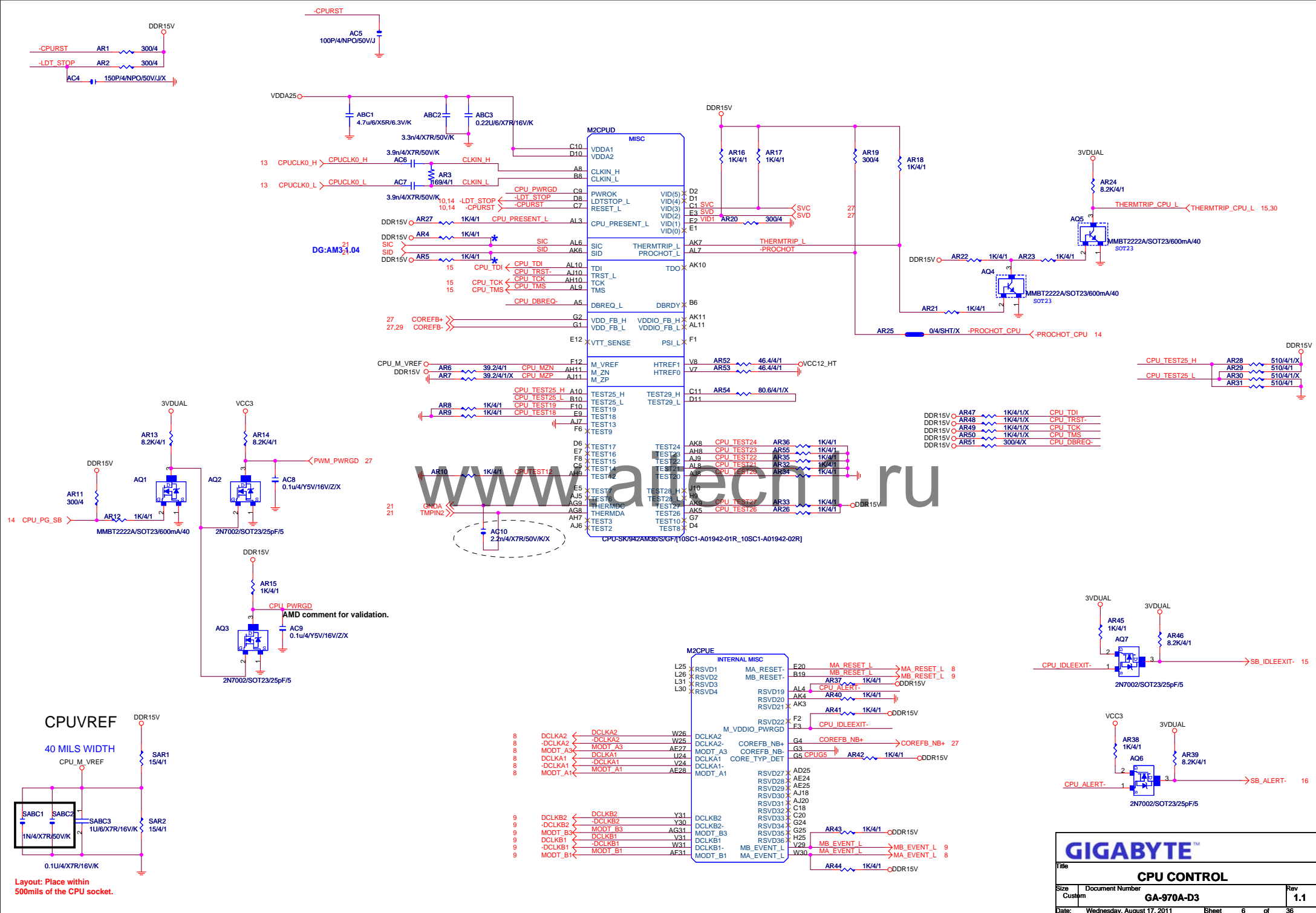


Figure 1: Schematic diagrams of the bottom side of the PCB.

The figure consists of three schematic diagrams arranged vertically, each representing a different layer of the PCB. The top diagram is labeled "BOTTOM SIDE" and shows a network of capacitors connected to a VCORE_NB supply and ground. The middle diagram is labeled "BOTTOM SIDE" and shows a network of capacitors connected to a DDR15V supply and ground. The bottom diagram is labeled "BOTTOM SIDE" and shows a network of capacitors connected to a VCORE supply and ground.

Top Diagram (Bottom Side):

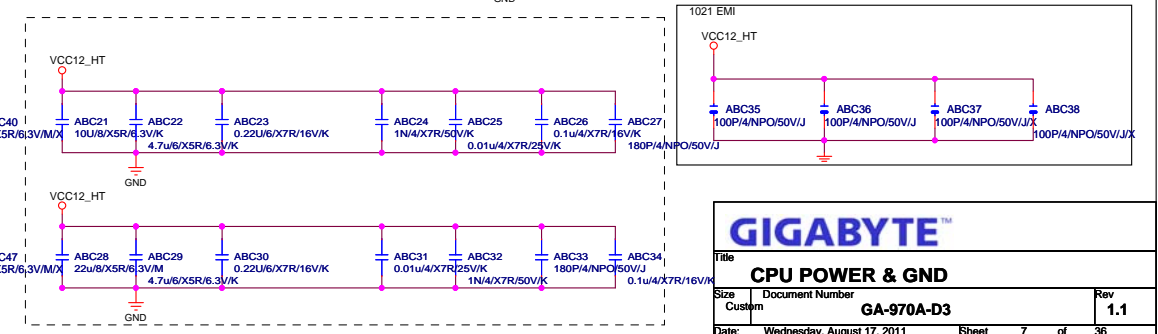
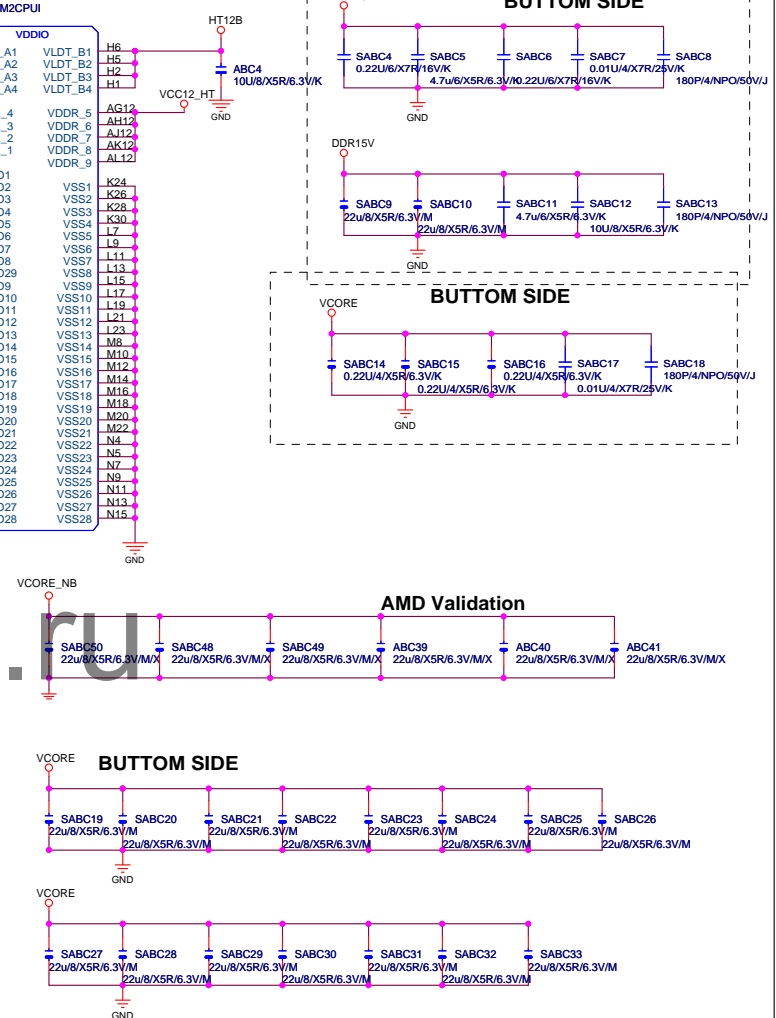
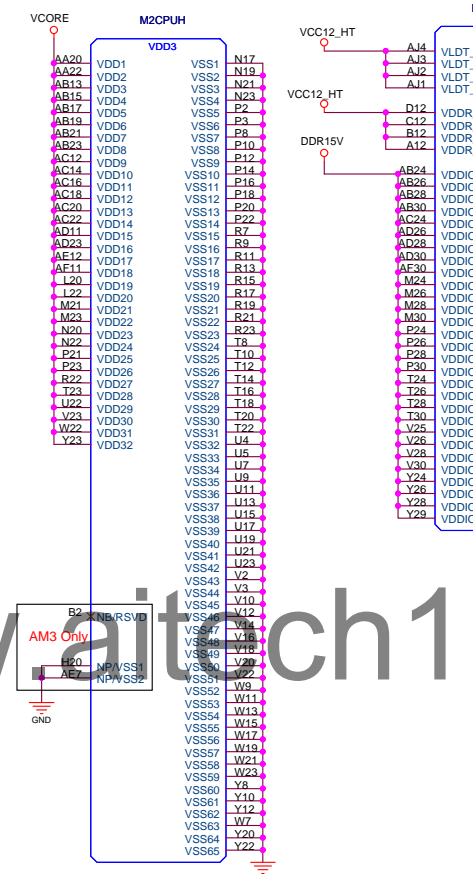
- Supply: VCORE_NB
- Ground: GND
- Capacitors: ABC5 (22u/8/X5R/6.3V/K), ABC6 (22u/8/X5R/6.3V/M), ABC7 (4.7u/6/X5R/6.3V/K), ABC8 (0.22u/4/X7R/16V/K), ABC9 (0.01u/4/X7R/25V/K), ABC10 (180P/4/NPO/50V/J)

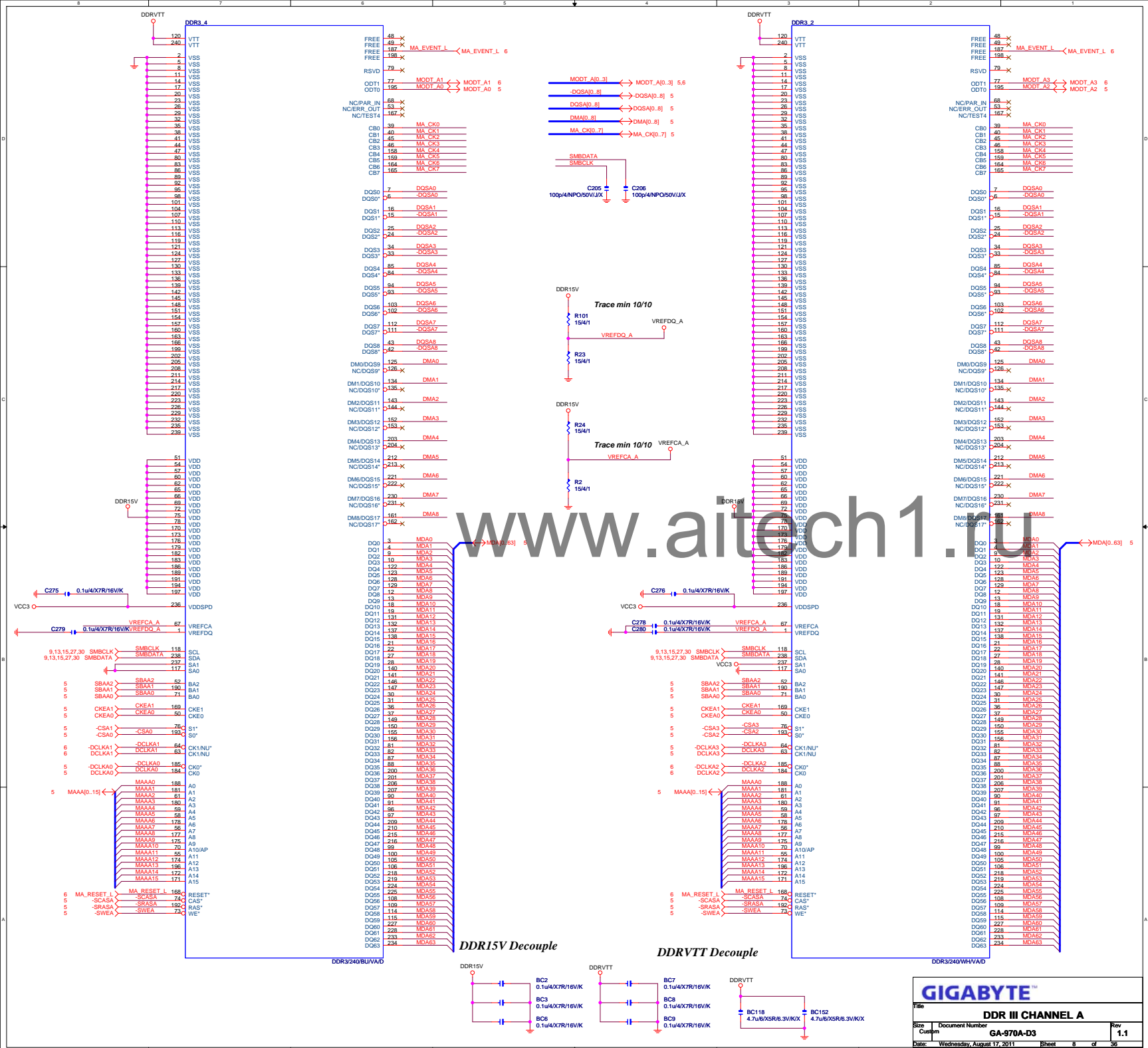
Middle Diagram (Bottom Side):

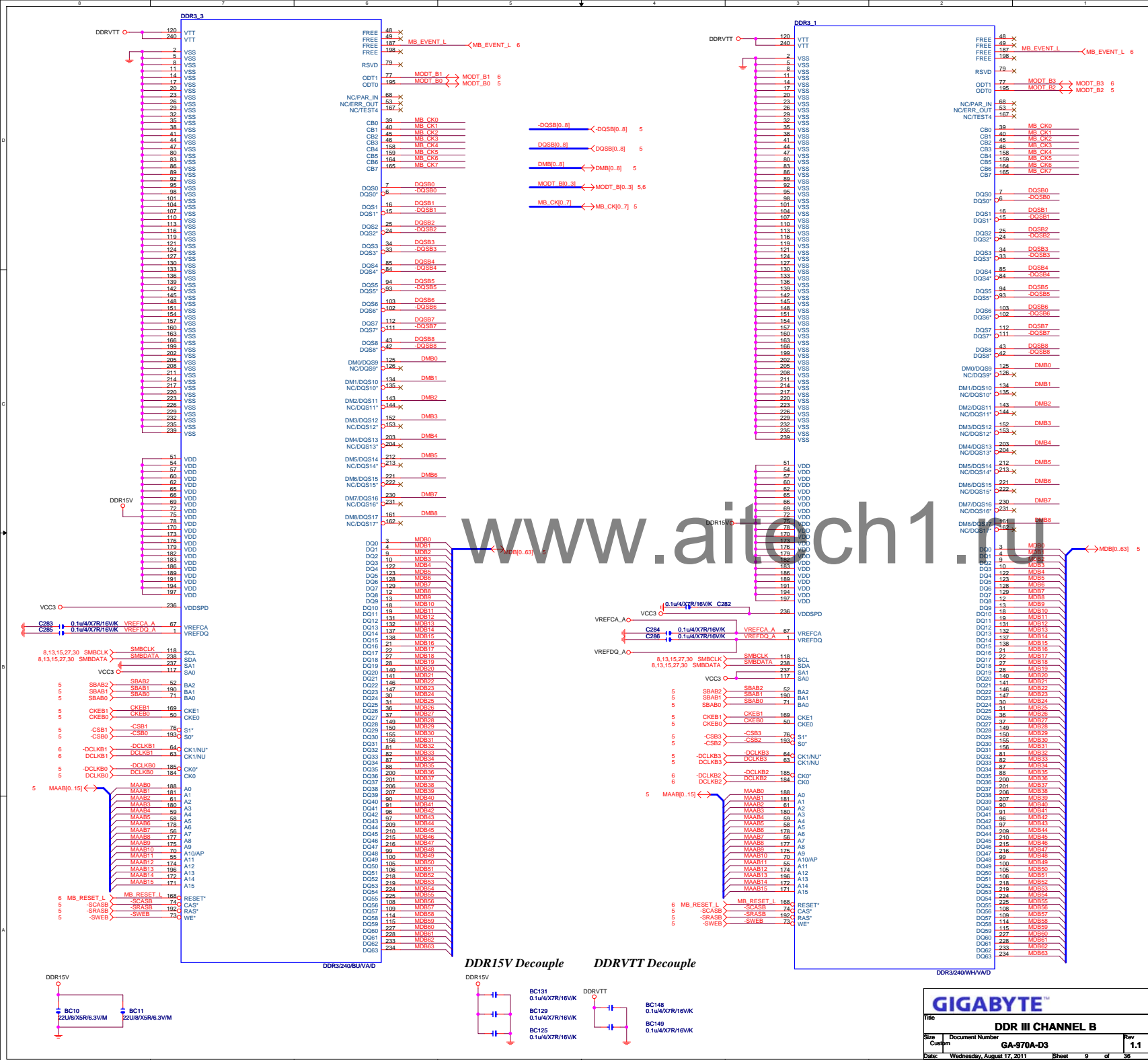
- Supply: DDR15V
- Ground: GND
- Capacitors: SABC4 (0.22u/6/X7R/16V/K), SABC5 (4.7u/6/X5R/6.3V/K), SABC6 (0.22u/4/X7R/16V/K), SABC7 (0.01u/4/X7R/25V/K), SABC8 (180P/4/NPO/50V/J)

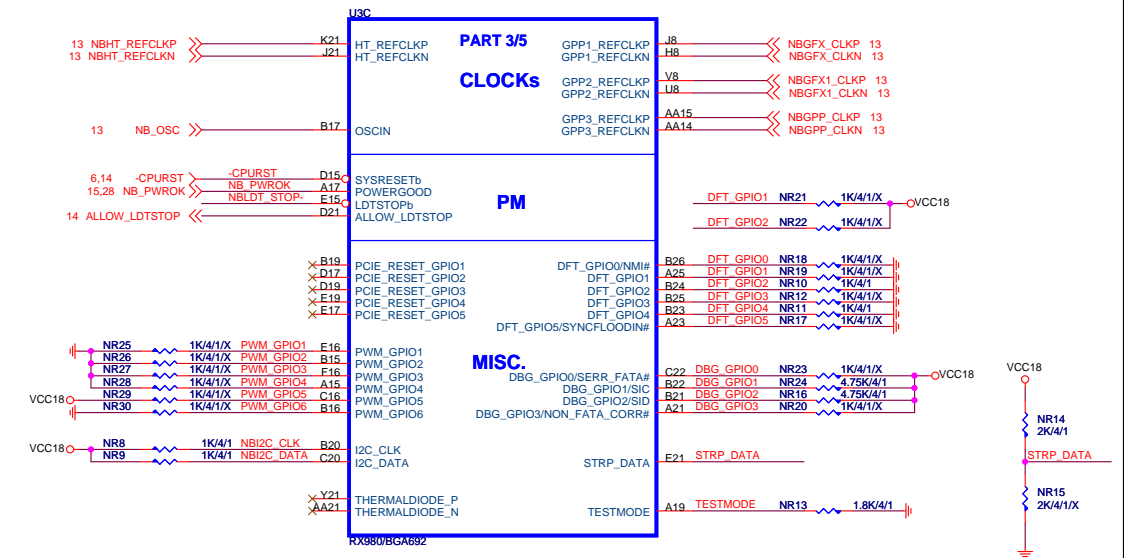
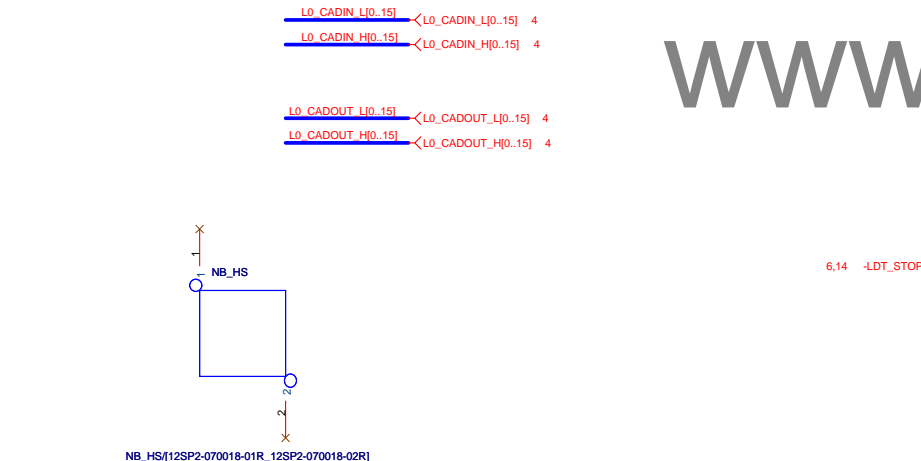
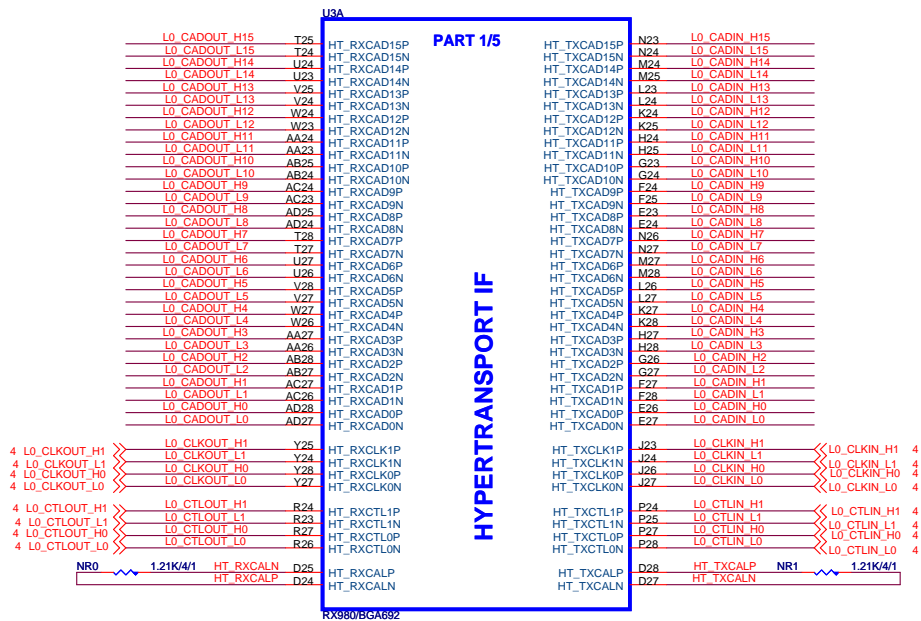
Bottom Diagram (Bottom Side):

- Supply: VCORE
- Ground: GND
- Capacitors: SABC14 (0.22u/4/X5R/6.3V/K), SABC15 (0.22u/4/X5R/6.3V/K), SABC16 (0.22u/4/X5R/6.3V/K), SABC17 (0.01u/4/X7R/25V/K), SABC18 (180P/4/NPO/50V/J)

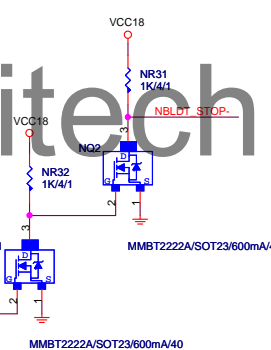








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DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.
GPIO4:3:2
000 : 4:2:4 B
001 : 4:1:1:4 C
010 : 1:1:1:1:1:4 L (Hardware Default)
011 : 2:1:1:1:1:4 E
100 : 2:2:1:1:4 K
101 : 2:2:2:4 C2
110: Hardware default (mode L) or EEPROM
111: Hardware default (mode L) or EEPROM
101 : 01100
111 : 01011

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLED

Enables the Test Debug Bus using PCIE bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable



U3B

PART 2/5

EXP A_RXP15 N6
EXP A_RXN15 N5
EXP A_RXP14 M4
EXP A_RXN14 L6
EXP A_RXP13 L5
EXP A_RXN13 K5
EXP A_RXP12 K4
EXP A_RXN12 J6
EXP A_RXP11 J5
EXP A_RXN11 H4
EXP A_RXP10 H4
EXP A_RXN10 G6
EXP A_RXP9 G5
EXP A_RXN9 F5
EXP A_RXP8 F4
EXP A_RXN8 D2
EXP A_RXP7 D1
EXP A_RXN7 B5
EXP A_RXP6 C5
EXP A_RXN6 D6
EXP A_RXP5 E6
EXP A_RXN5 E7
EXP A_RXP4 F7
EXP A_RXN4 D8
EXP A_RXP3 E8
EXP A_RXN3 F9
EXP A_RXP2 F9
EXP A_RXN2 D10
EXP A_RXP1 E10
EXP A_RXN1 E11
EXP A_RXP0 F11
EXP A_RXN0 F11

PCIE GPP1

GPP1_RX15P N3
GPP1_RX15N M2
GPP1_RX14P M1
GPP1_TX14N L3
GPP1_TX13P L2
GPP1_TX13N K1
GPP1_TX12P J3
GPP1_TX12N J2
GPP1_RX11P H2
GPP1_TX11N H1
GPP1_TX10P G3
GPP1_TX10N G2
GPP1_TX9P F2
GPP1_TX9N F1
GPP1_TX8P E3
GPP1_TX8N E2
GPP1_TX7P A4
GPP1_TX7N B4
GPP1_TX6P A6
GPP1_TX6N B6
GPP1_TX5P B7
GPP1_TX5N C7
GPP1_TX4P A8
GPP1_TX4N B8
GPP1_TX3P B9
GPP1_TX3N C9
GPP1_TX2P A10
GPP1_TX2N B10
GPP1_TX1P B11
GPP1_TX1N C11
GPP1_TX0P
GPP1_TX0N

AC9
AD9
AE8
AE7
AD7
AD6
AE6
AF5
AG5
AF2
AD2
AD1
AB5
AA6
AA5
Y5
Y4
W6
W5
V5
V4
U6
U5
T5
T4
R6
R5
P5
P4

PCIE GPP2

GPP2_RX15P AF9
GPP2_RX15N AG9
GPP2_RX14P AG8
GPP2_TX14N AH8
GPP2_TX13P AF7
GPP2_TX13N AG7
GPP2_TX12P AG6
GPP2_TX12N AH6
GPP2_TX11P AG4
GPP2_TX11N AH4
GPP2_TX10P AE3
GPP2_TX10N AE2
GPP2_TX9P AC3
GPP2_TX9N AC2
GPP2_TX8P AB2
GPP2_TX8N AB1
GPP2_TX7P AA3
GPP2_TX7N AA2
GPP2_TX6P Y2
GPP2_TX6N Y1
GPP2_TX5P W3
GPP2_TX5N W2
GPP2_TX4P V2
GPP2_TX4N V1
GPP2_TX3P U2
GPP2_TX3N U1
GPP2_TX2P T2
GPP2_TX2N T1
GPP2_TX1P R3
GPP2_TX1N R2
GPP2_TX0P P2
GPP2_TX0N P1

AD11
AC11
AE12
AD12
AD13
AC13
AE14
AD14
AD15
AC15
AE16
AD16
AD17
AC17
AE18
AD18
AD19
AC19
AH20
AG20

PCIE GPP3

GPP3_RX9P AH19
GPP3_RX9N AG19
GPP3_TX8P AE11
GPP3_TX8N AE12
GPP3_TX7P AH12
GPP3_TX7N AG12
GPP3_TX6P AE13
GPP3_TX6N AE14
GPP3_TX5P AG14
GPP3_TX5N AG15
GPP3_TX4P AE16
GPP3_TX4N AE17
GPP3_TX3P AG18
GPP3_TX3N AG19
GPP3_TX2P AE17
GPP3_TX2N AE18
GPP3_TX1P AG18
GPP3_TX1N AG19
GPP3_TX0P AE19
GPP3_TX0N AE19

PCI_E slot TX need CAP close to slot side

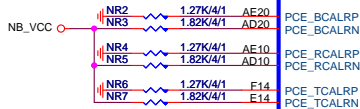
AC21
AD21
AE22
AF25
AG25
AG26
AH26

PCIE ALINK

SB_RX3P AG22
SB_RX3N AG21
SB_RX2P AG21
SB_RX2N AF23
SB_RX1P AG23
SB_RX1N AG24
SB_RX0P AH24
SB_RX0N

AG22 A_TX3P C NC11 0.1u/4/X7R/16V/K A_TX3P 14
AH22 A_TX3N C NC12 0.1u/4/X7R/16V/K A_TX3N 14
AE21 A_TX2P C NC14 0.1u/4/X7R/16V/K A_TX2P 14
AG21 A_TX2N C NC13 0.1u/4/X7R/16V/K A_TX2N 14
AF23 A_TX1P C NC15 0.1u/4/X7R/16V/K A_TX1P 14
AG23 A_TX1N C NC16 0.1u/4/X7R/16V/K A_TX1N 14
AG24 A_TX0P C NC18 0.1u/4/X7R/16V/K A_TX0P 14
AH24 A_TX0N C NC17 0.1u/4/X7R/16V/K A_TX0N 14

PLACE THESE CAP CLOSE TO NB.



RX980/BGA692

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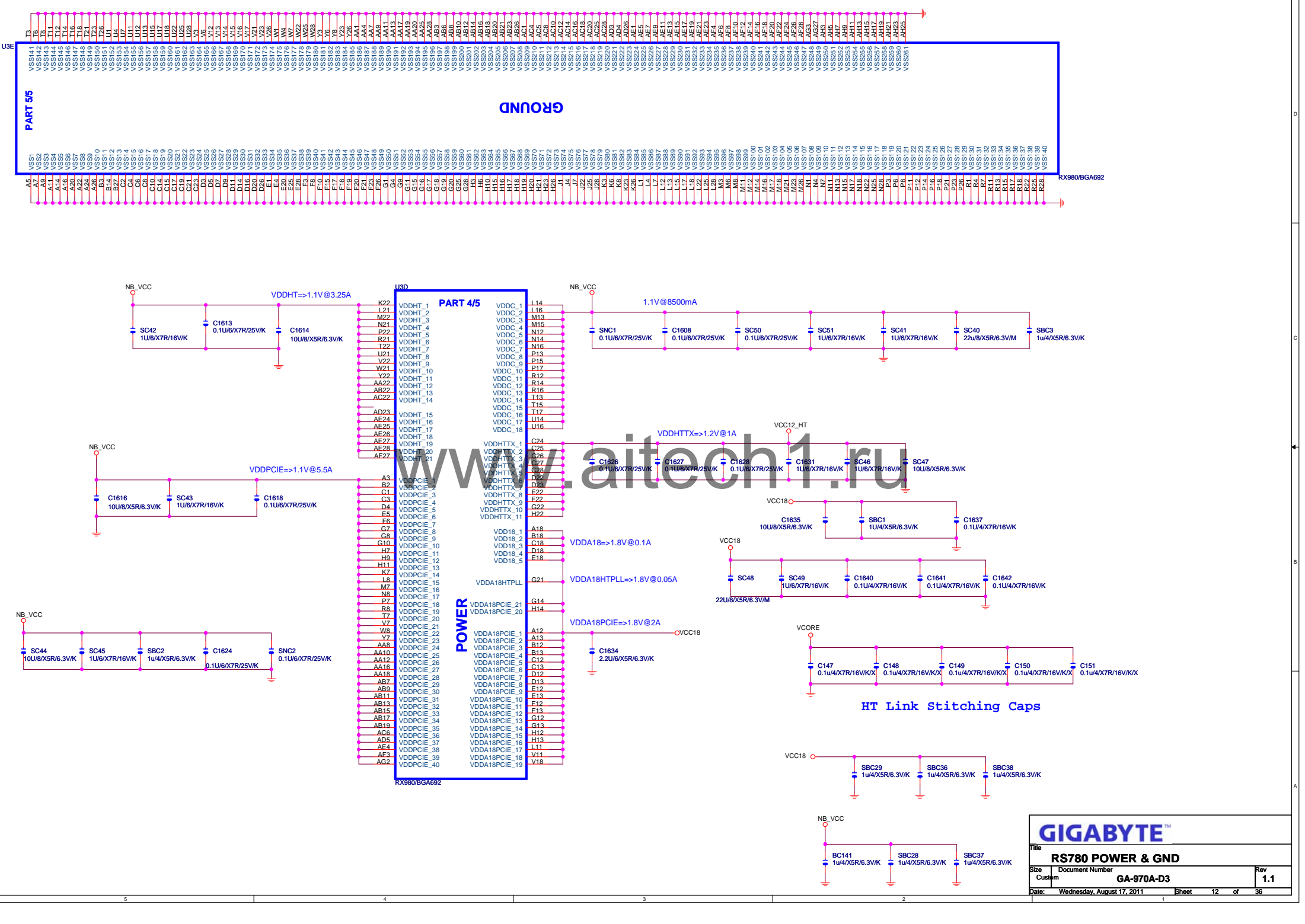
EXP A_TXP[0..15] >> EXP_A_TXP[0..15] 18
EXP A_TXN[0..15] >> EXP_A_TXN[0..15] 18
EXP A_RXP[0..15] >> EXP_A_RXP[0..15] 18
EXP A_RXN[0..15] >> EXP_A_RXN[0..15] 18

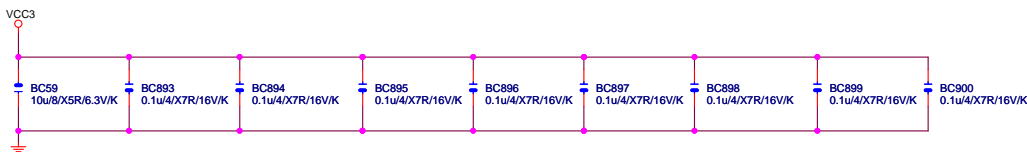
GIGABYTE™

Title RS780 PCIE I/F ,Switch

Size Custom Document Number GA-970A-D3 Rev 1.1

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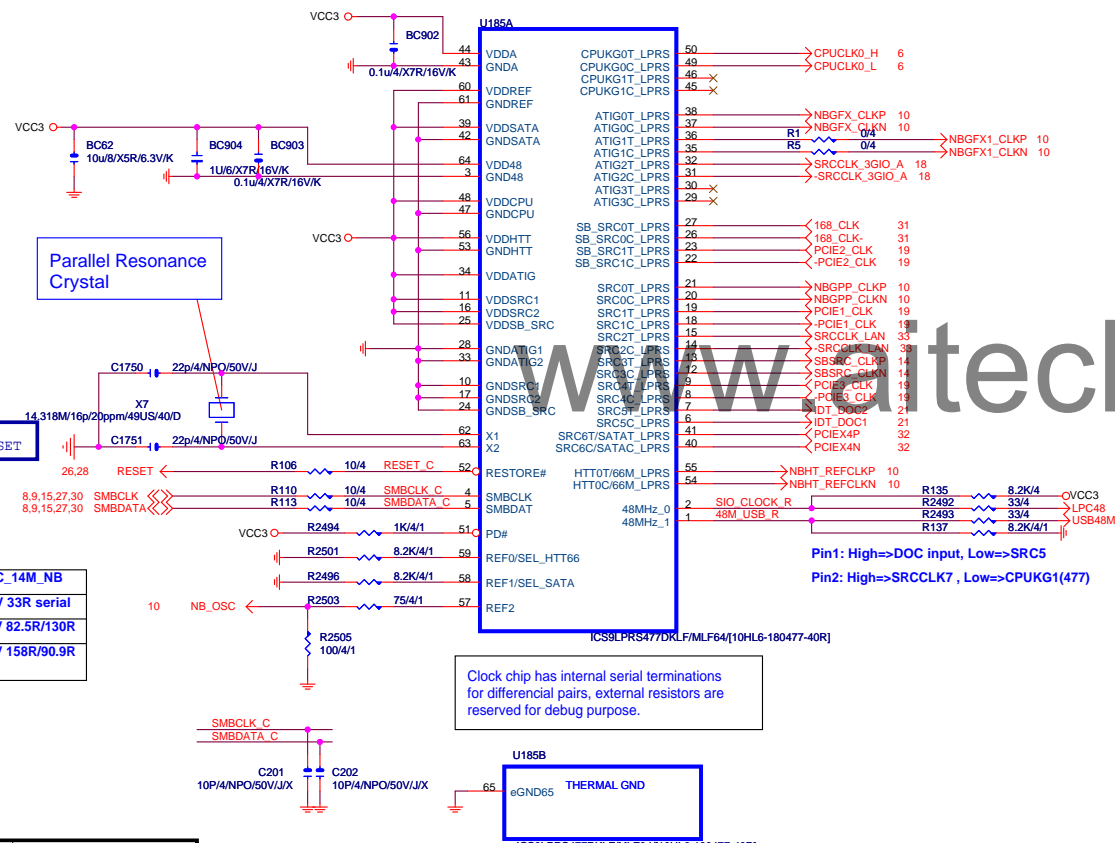
- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

Place R800/801 less than 500 mills away from U800
R851 less than 100 mills away from R800/801
route CPU clock as 100ohm differential pair

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases



	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB850

S.B HEATSINK

SB_HS

SB_HS(12SP2-S05110-01R_12SP2-S05110-02R_12SP2-S05110-03R)

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Low: Force PCIE GEN1, Up: Allow PCIE GEN2

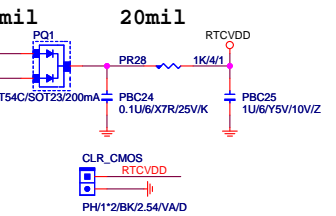
PULL HIGH PULL LOW

PULL HIGH PULL LOW

BIOS after boot setting
EC AOD-ACC

LPC CLK0 Rev.A12

LPC_CLK1



CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

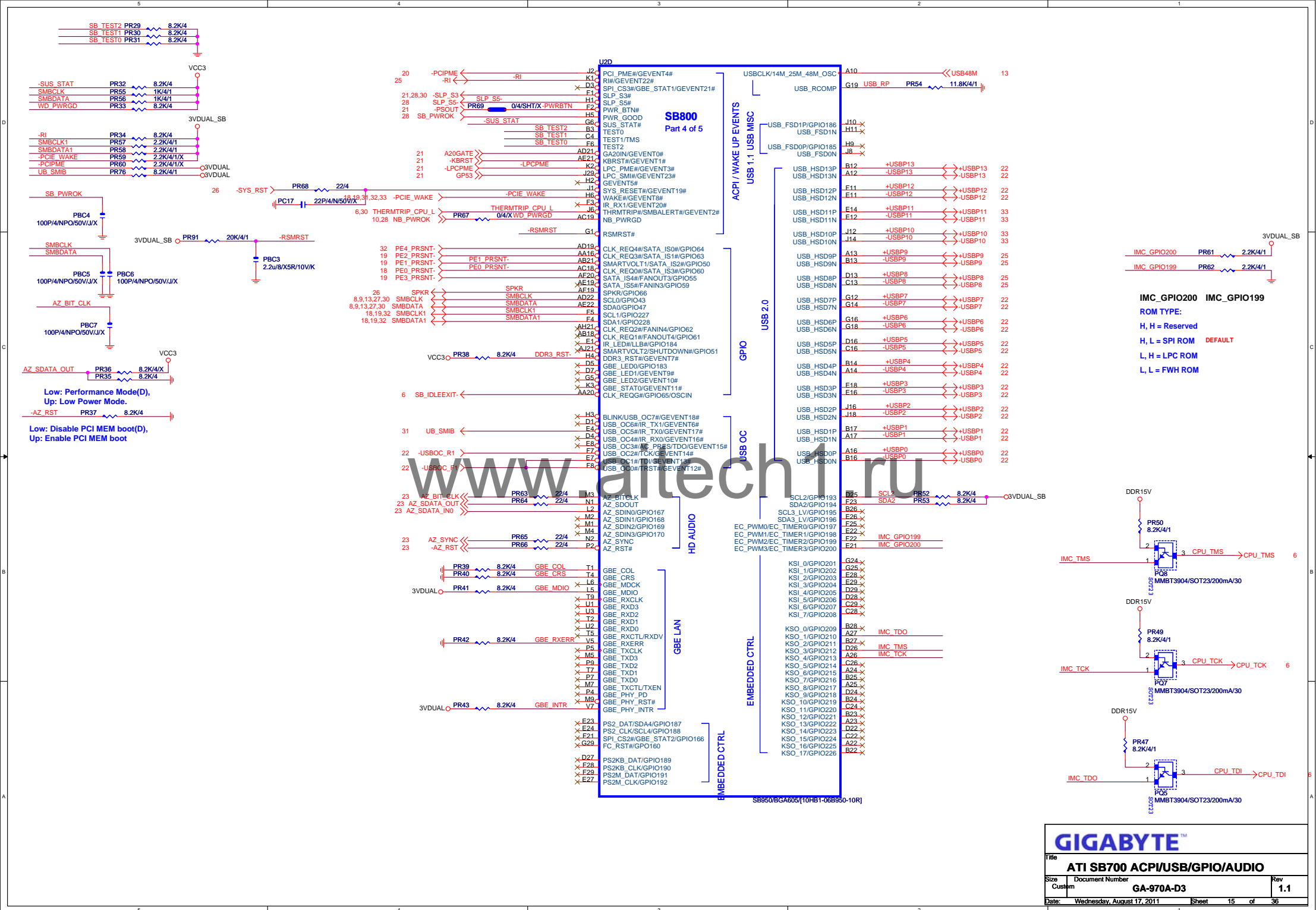
NOT ADD ICT FOR RTCVDD PIN

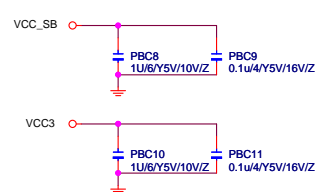
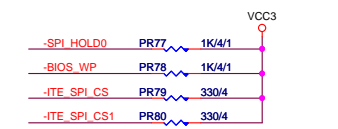
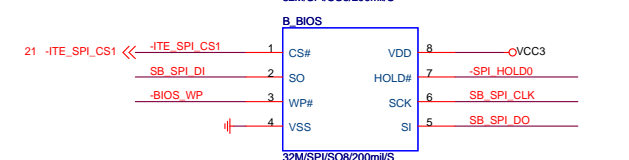
GIGABYTE

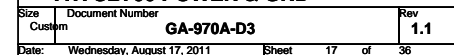
ATI SB700 PCIE/PCI/CPU/LPC

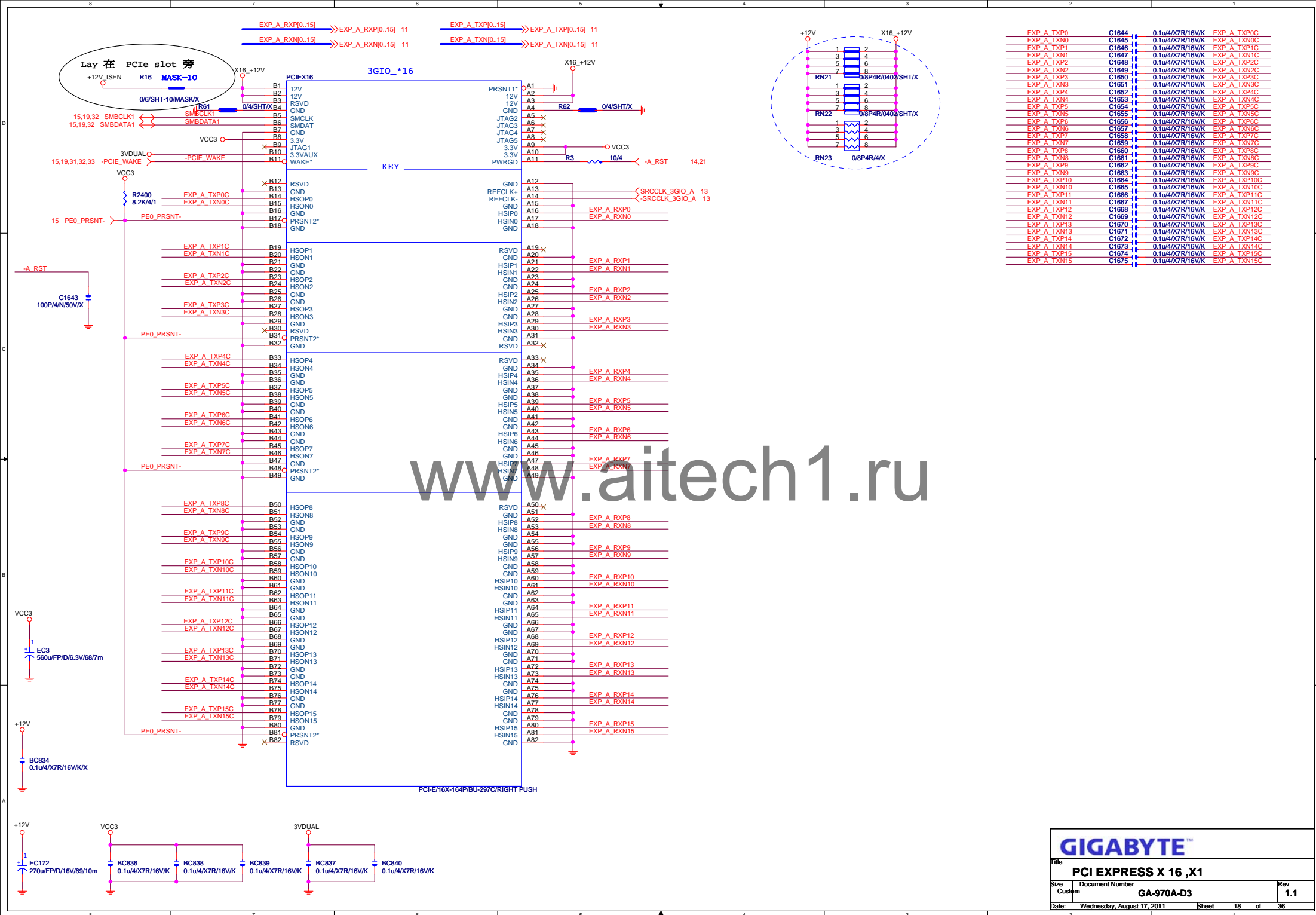
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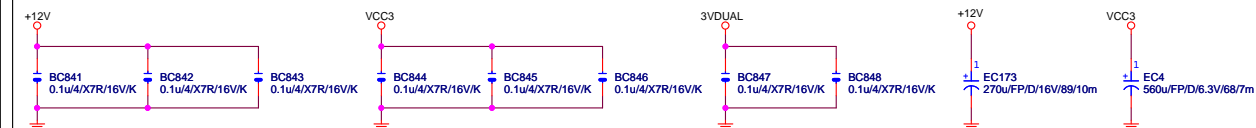
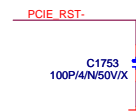
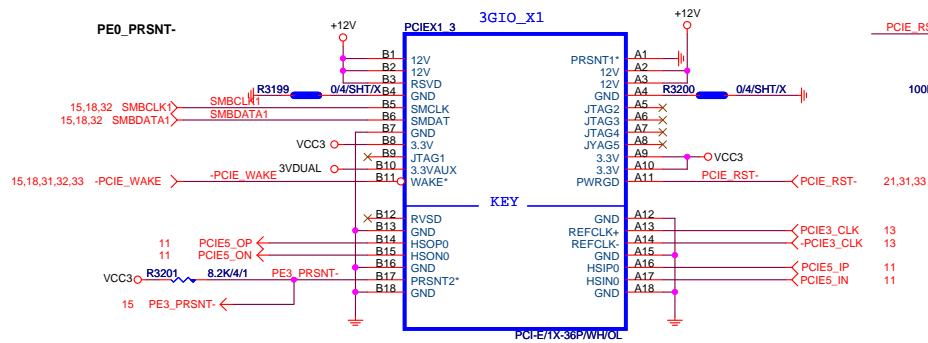
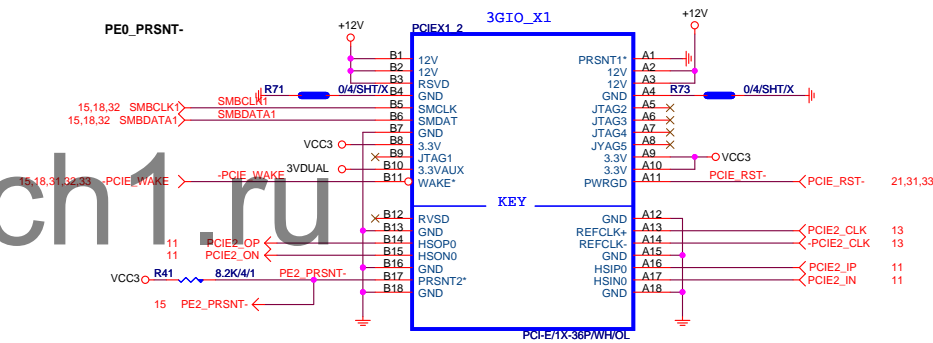
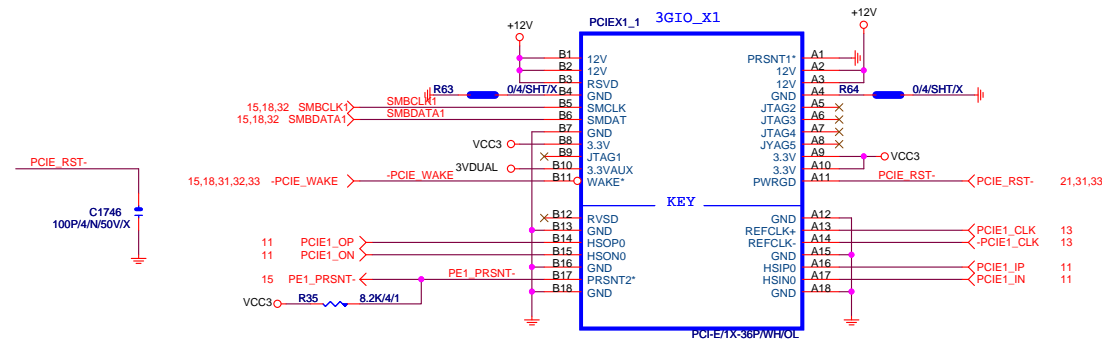




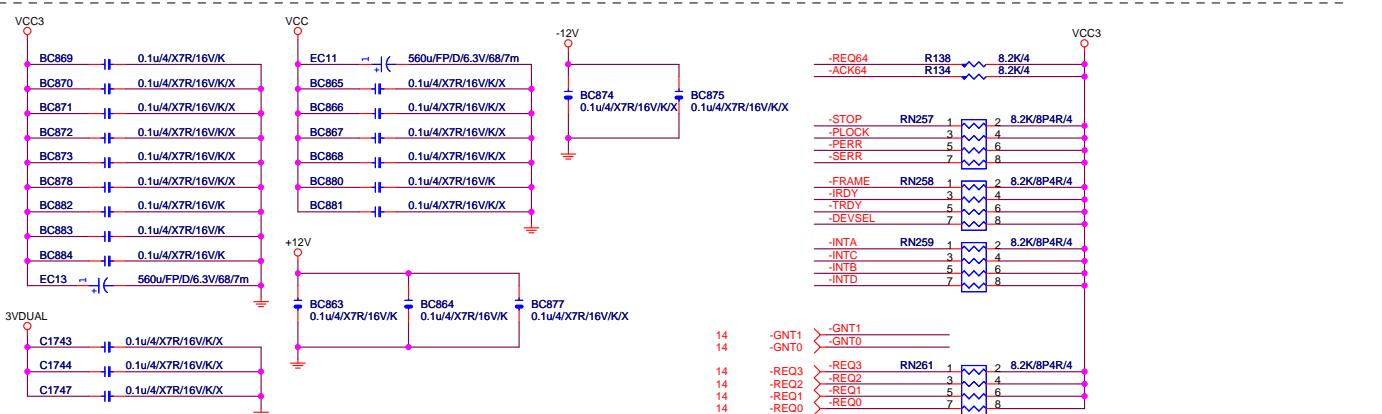
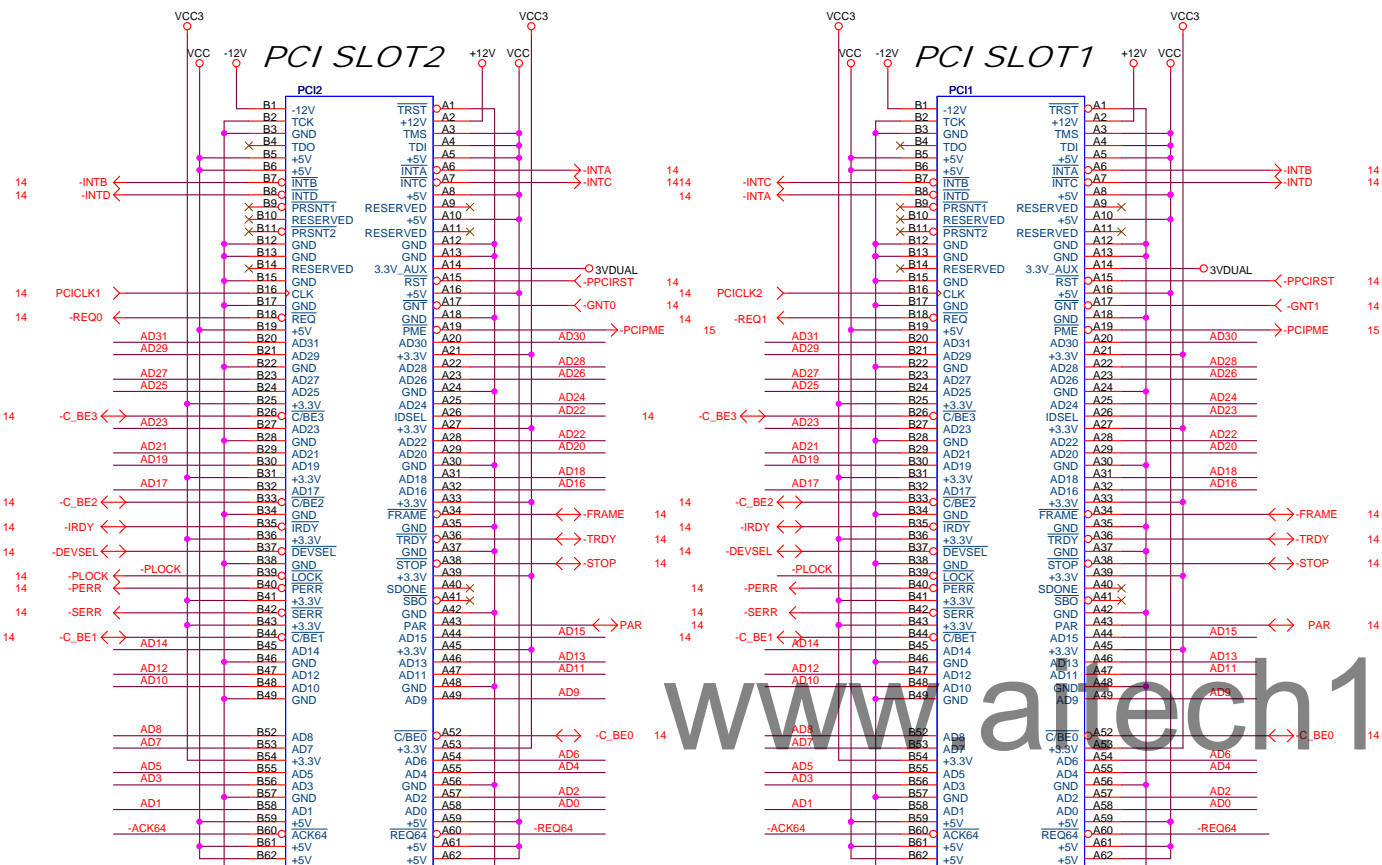


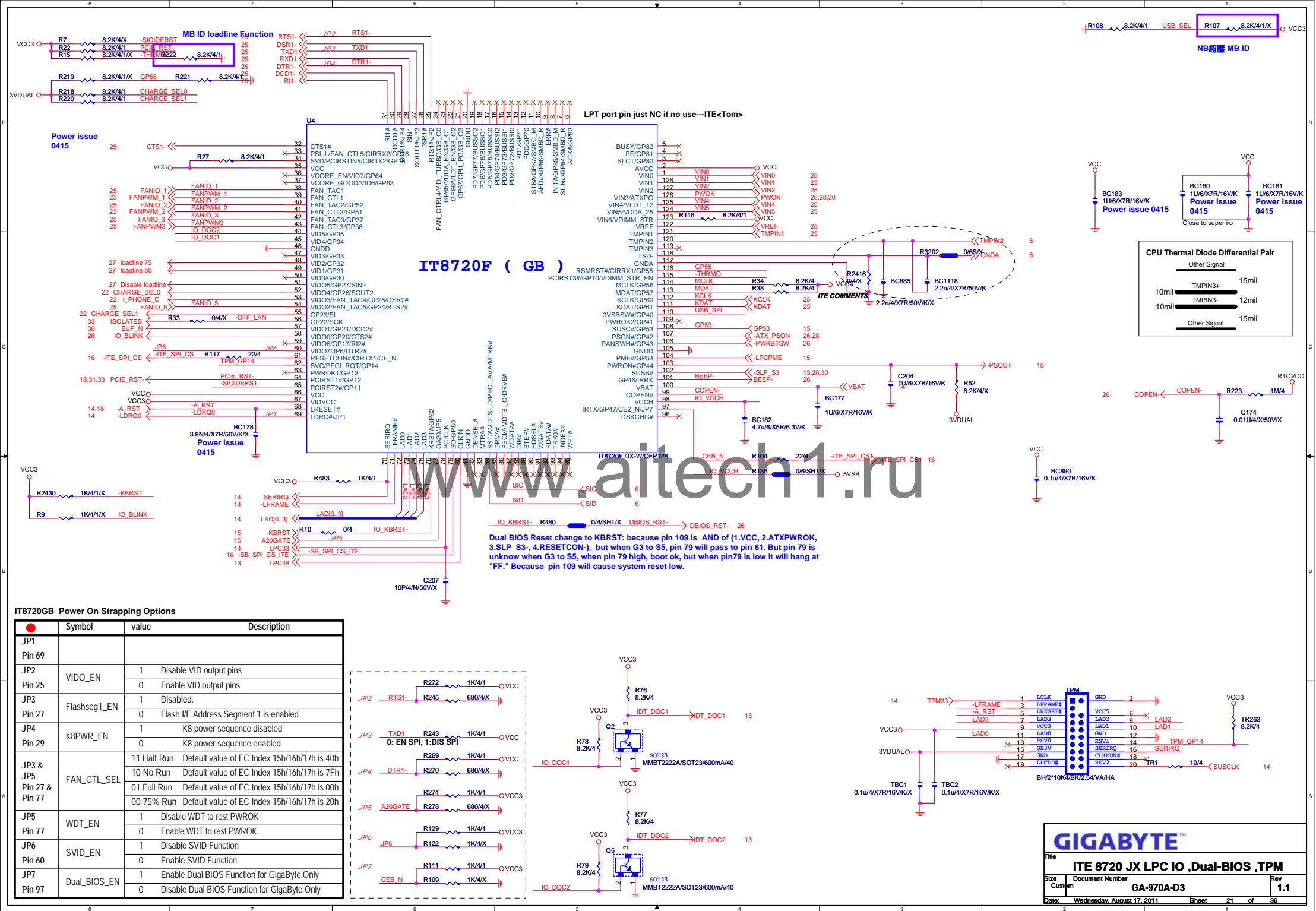


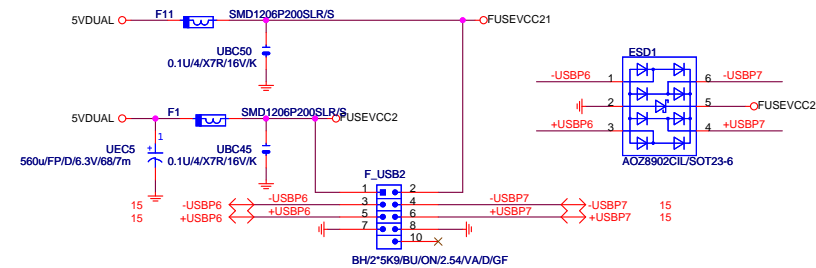
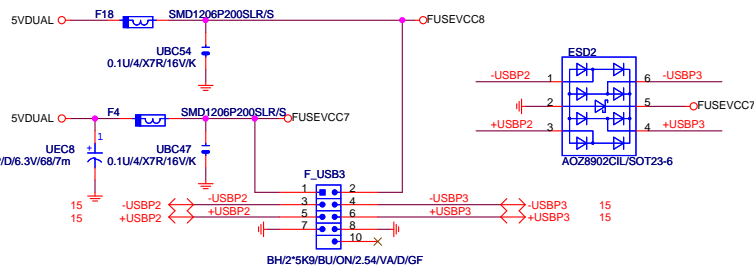
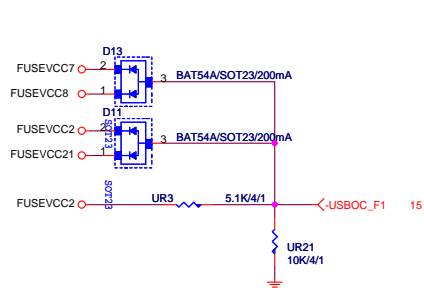
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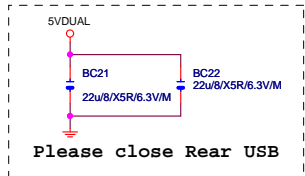
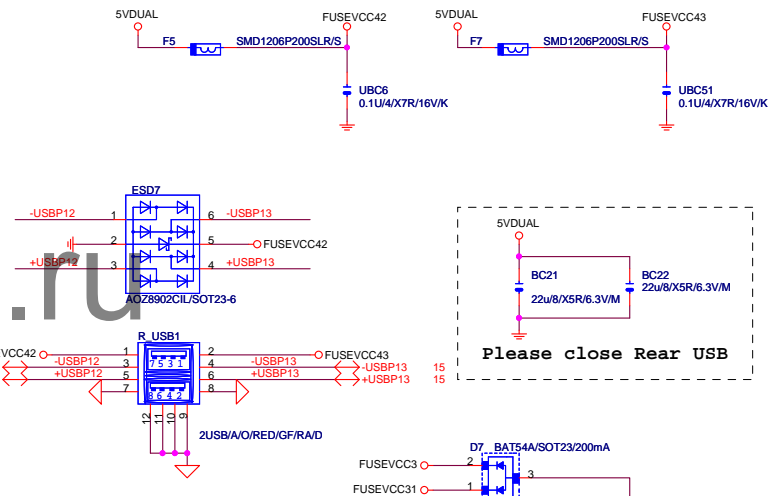
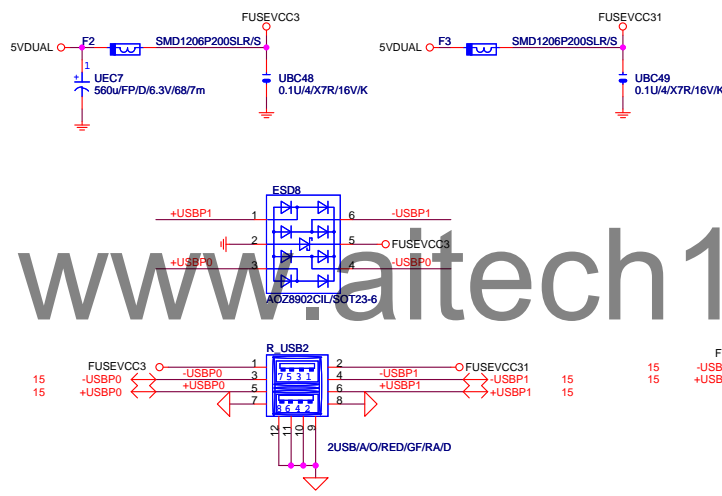
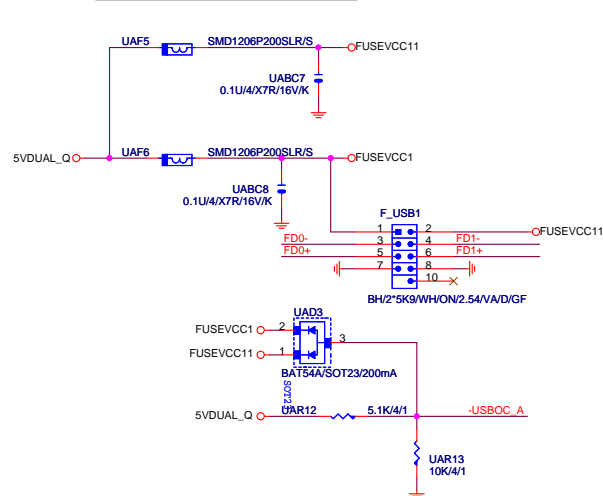
PCI SLOT 1,2



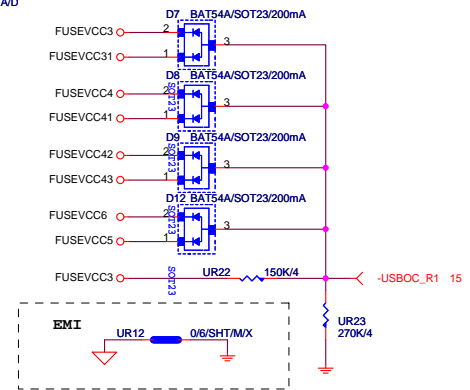




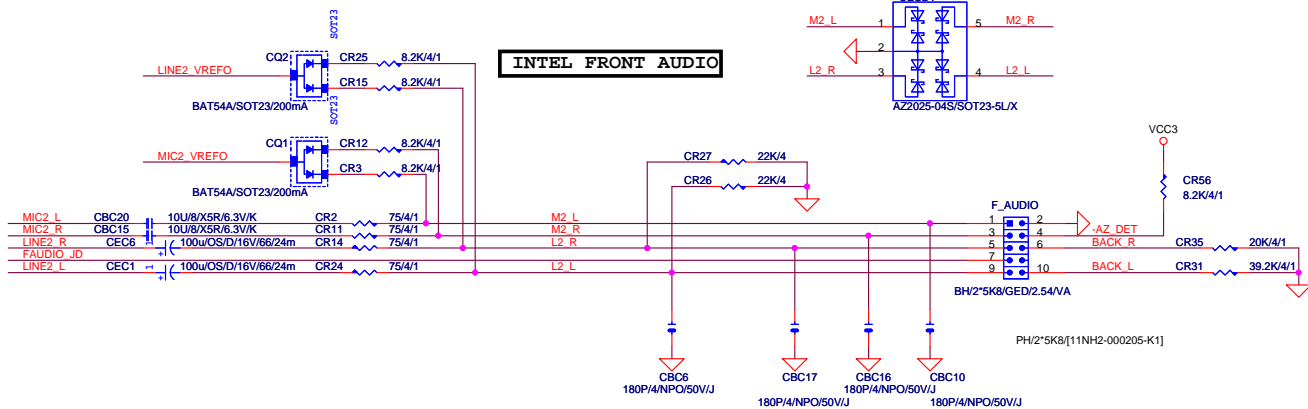
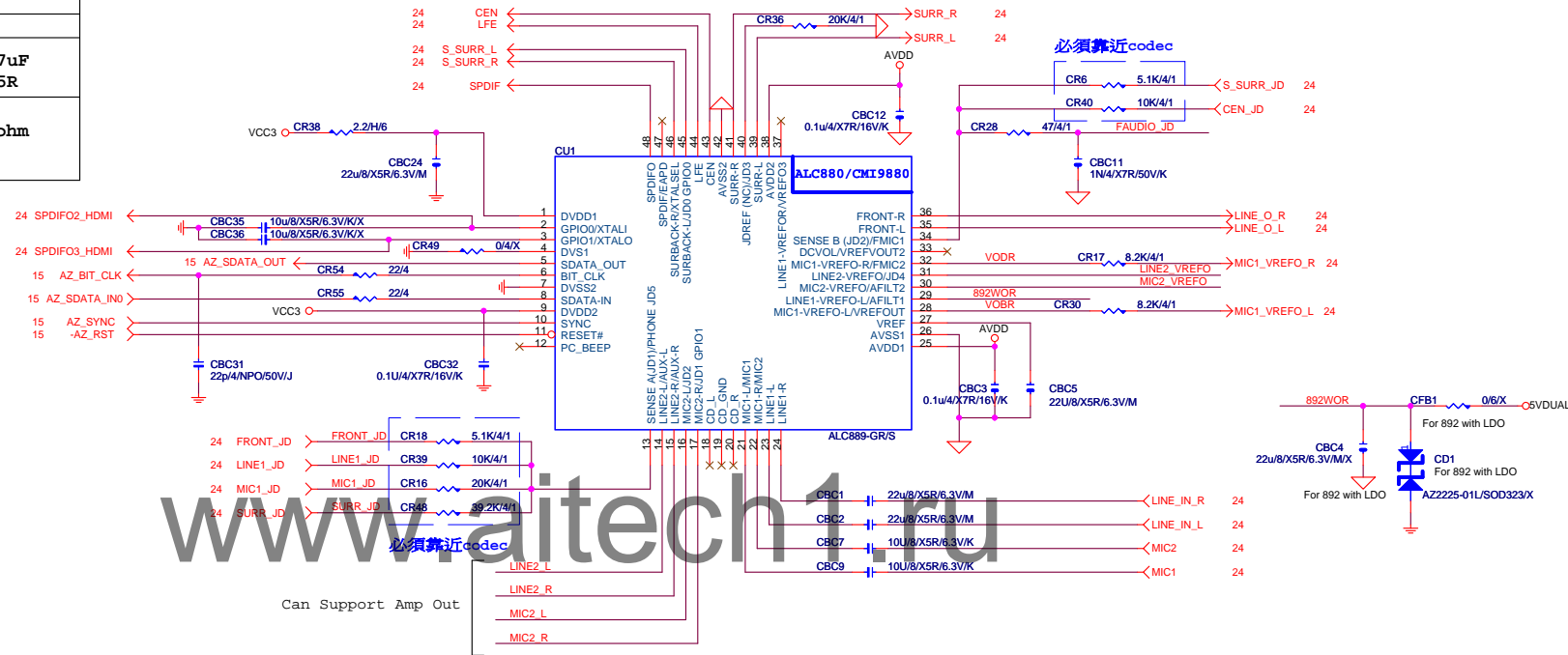
FRONT SIDE USB1

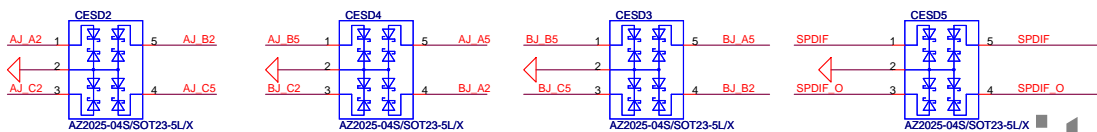
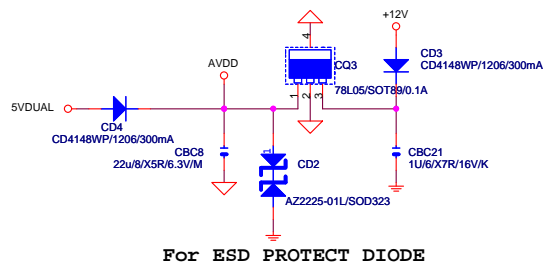
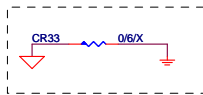


Please close Rear USB

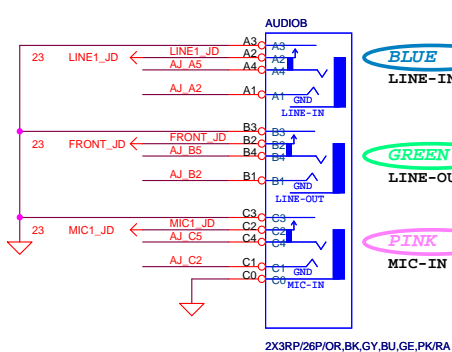
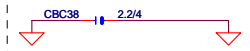


	ALC892R	ALC889	ALC889A
CR16	X	X	O
CR24	X	X	O
CR25	X	O	O
CBC42	10uF/X5R	X	X
CR2	20K/1%	20K/1%	20K/0.1%
CR9	O	O	X
CR10	X	X	O
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R	10uF /X5R	4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR27/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm	66 ohm or lower	75 ohm



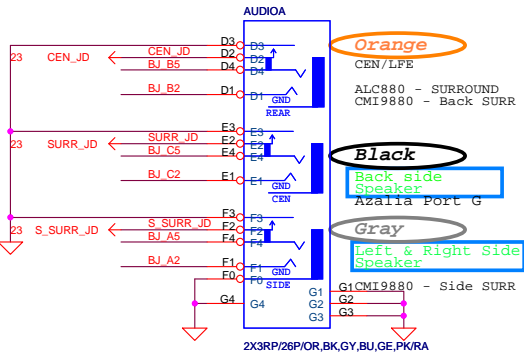
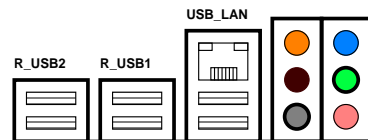
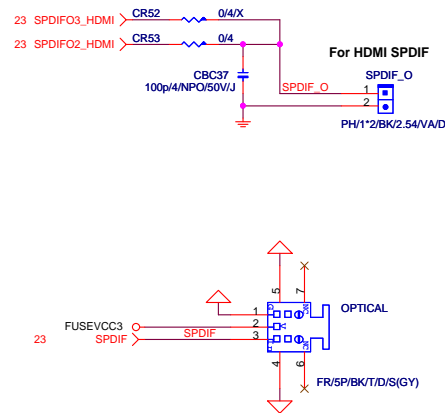


For Audio precision test



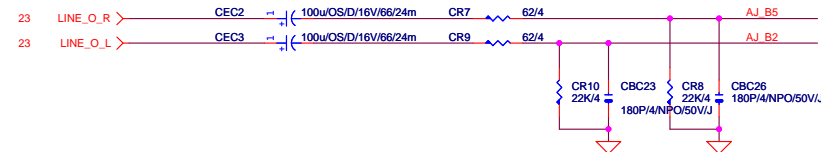
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3RJ*15P/[11NR6-403004-11]

SPDIF

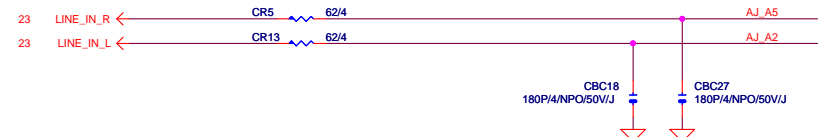


A3RJ/13P/0BG/[11NR6-403006-71]
3RJ*15P/[11NR6-403004-31]

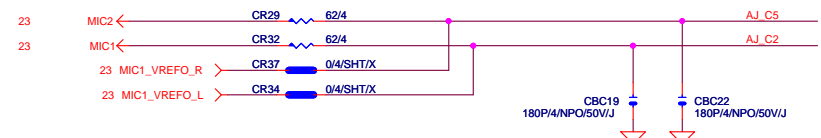
LINE OUT FRONT OUT



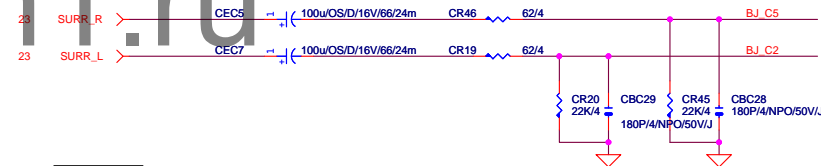
LINE-IN



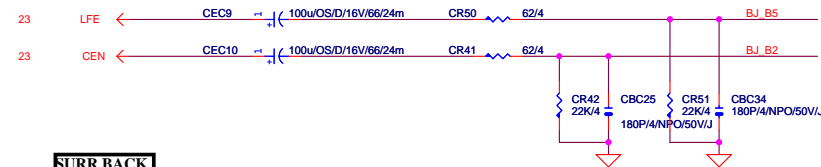
MIC



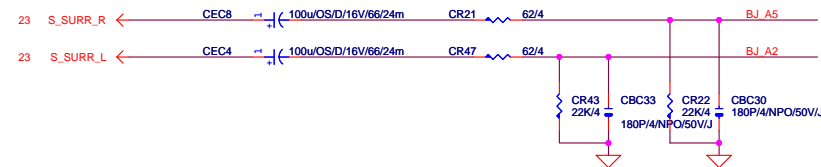
SURROUND



CEN/LFE



SURR BACK

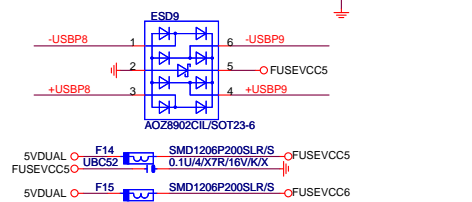
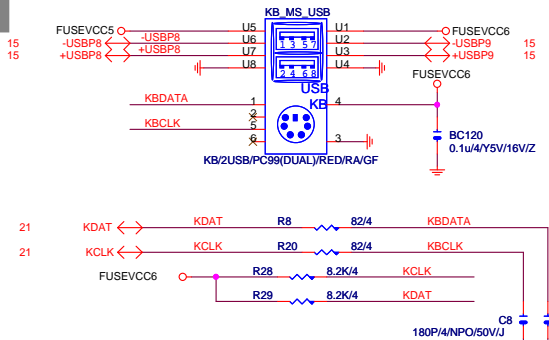
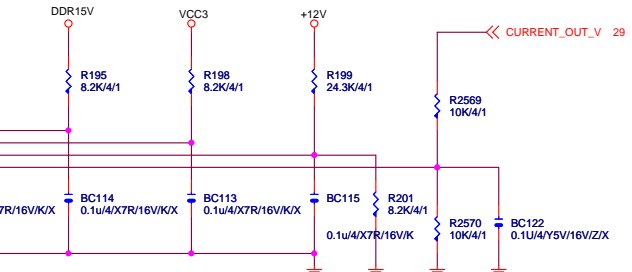
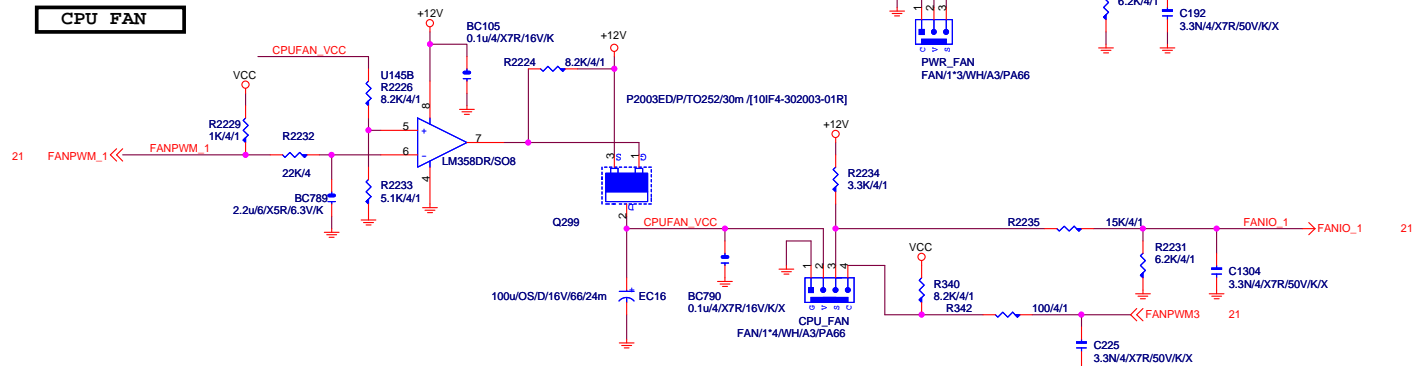
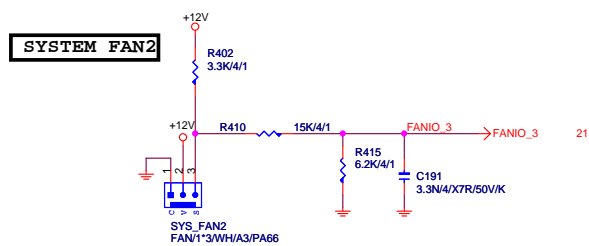
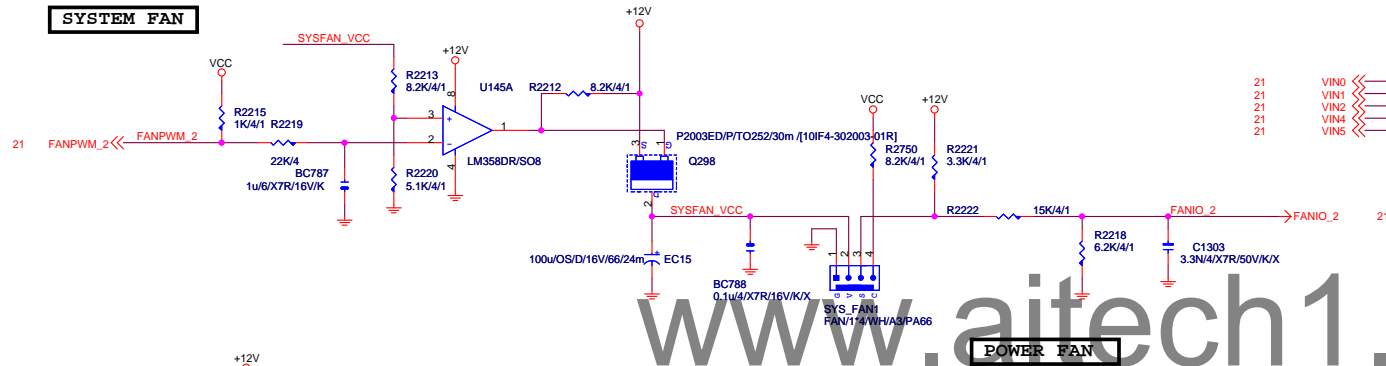
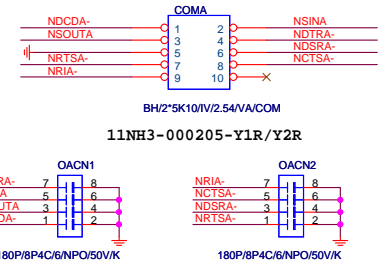
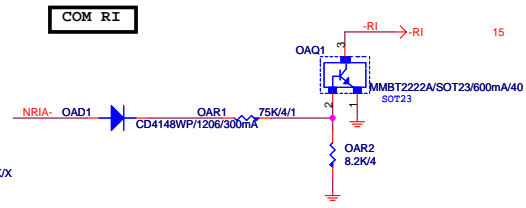
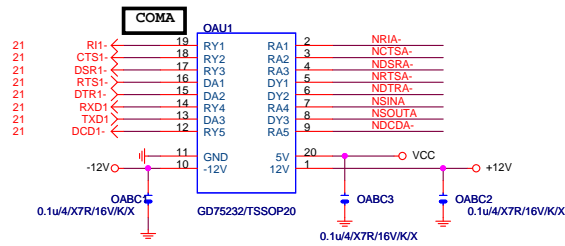
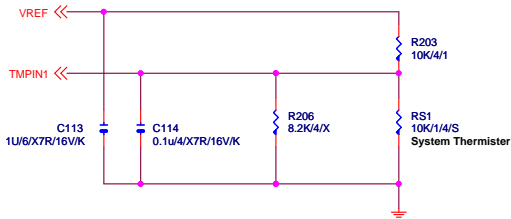


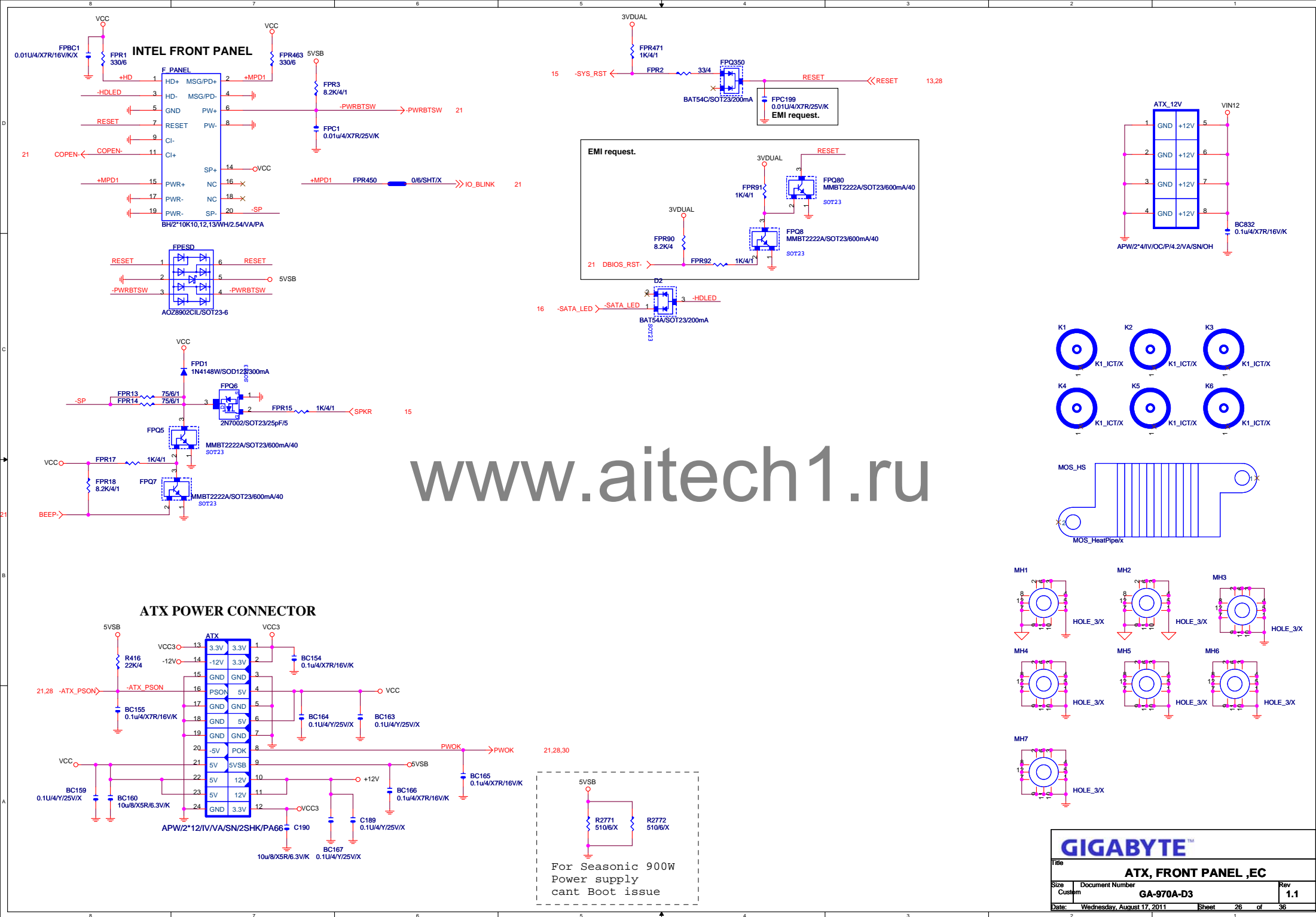
GIGABYTE

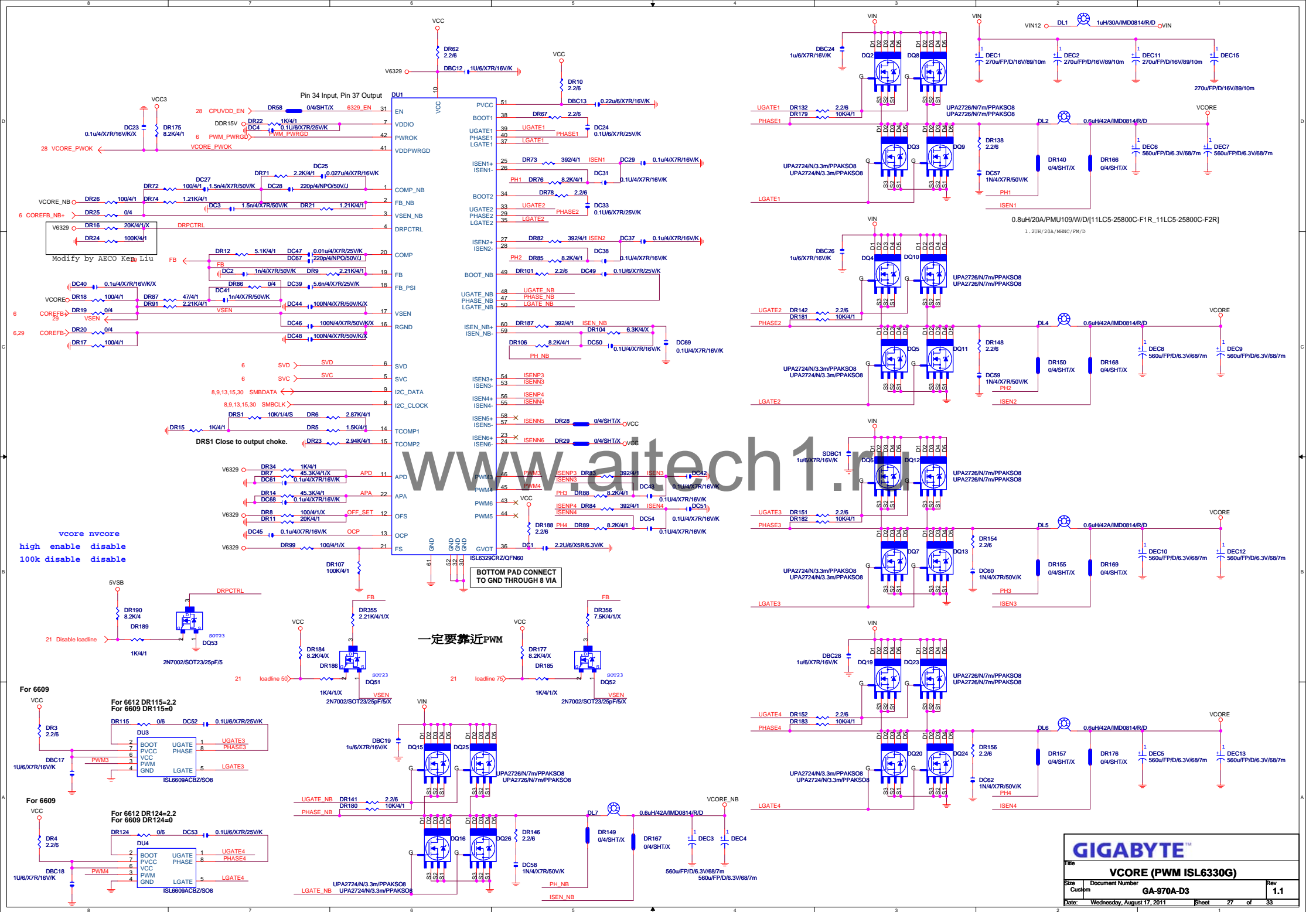
AUDIO JACK

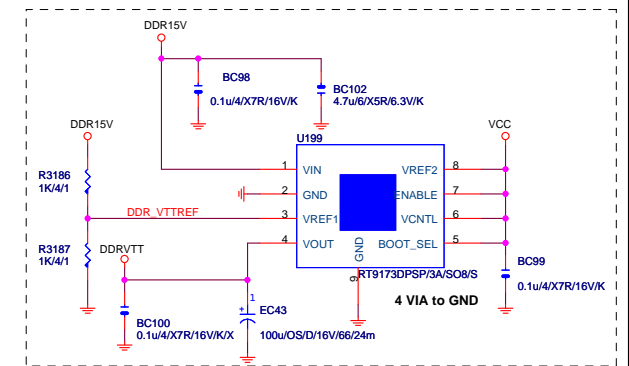
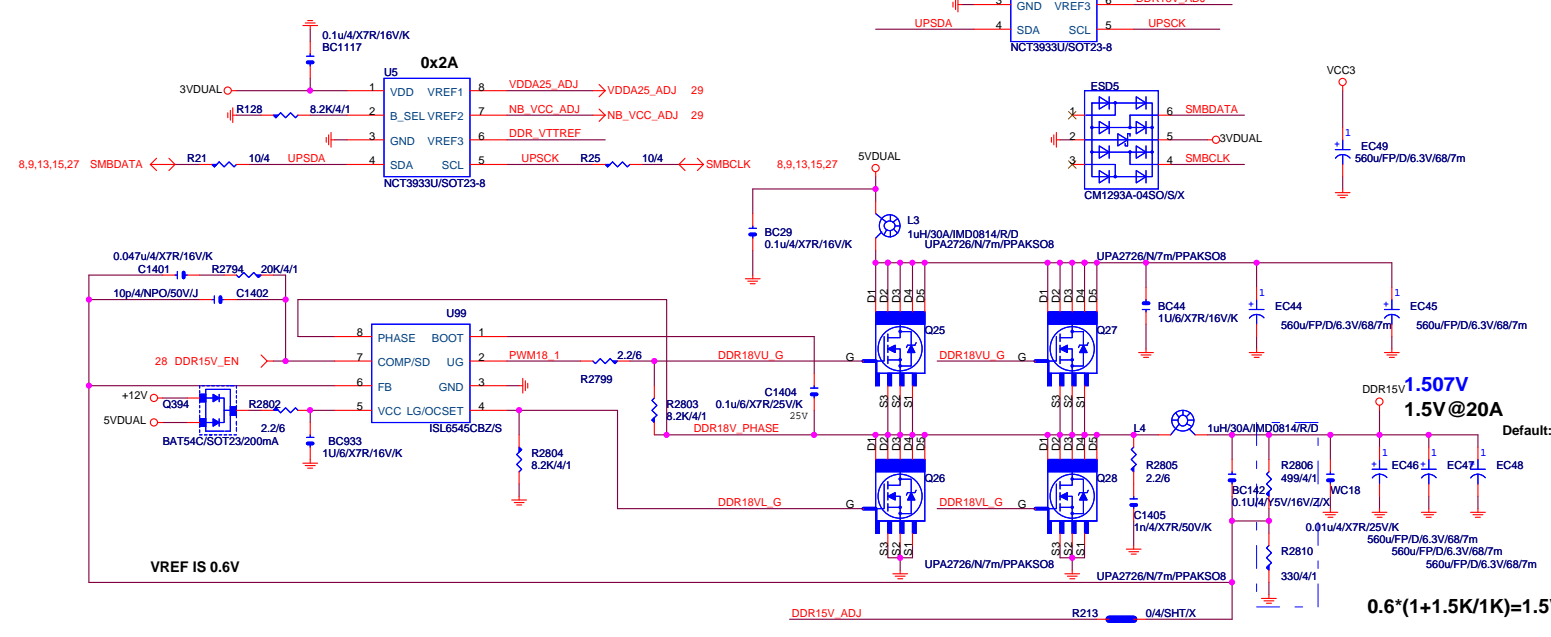
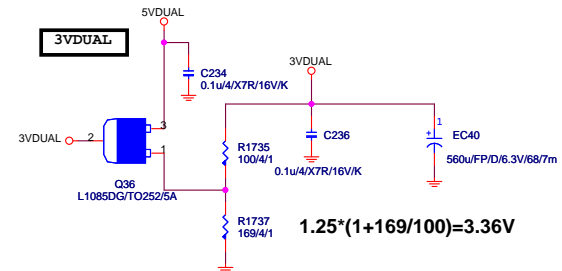
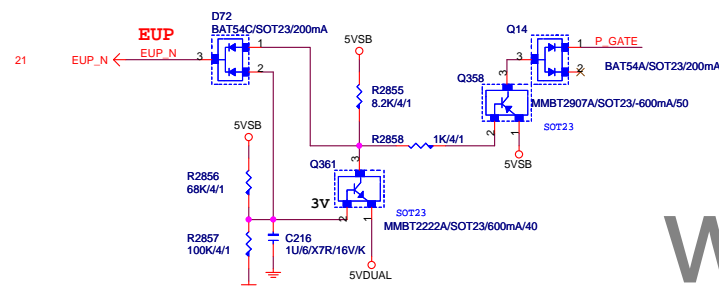
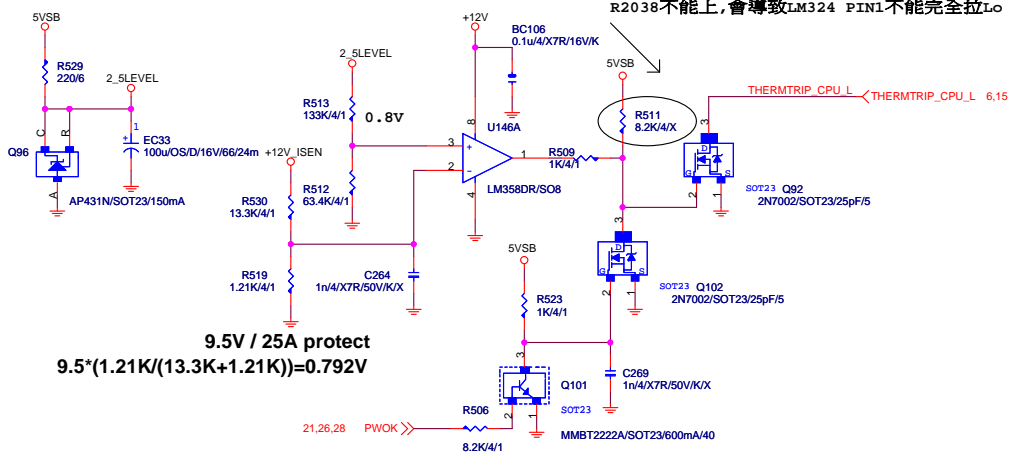
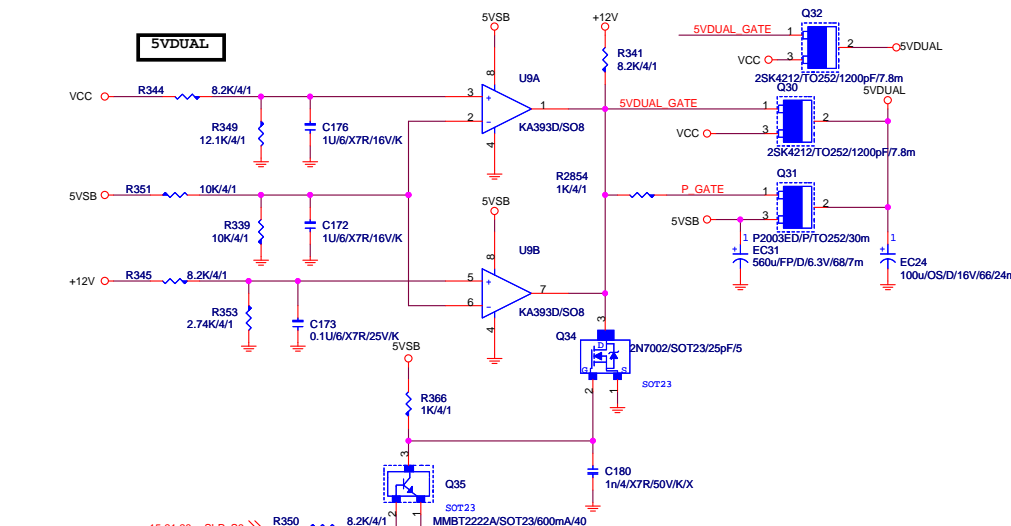
Size Custom
Date: Wednesday, August 17, 2011
Sheet 24 of 36

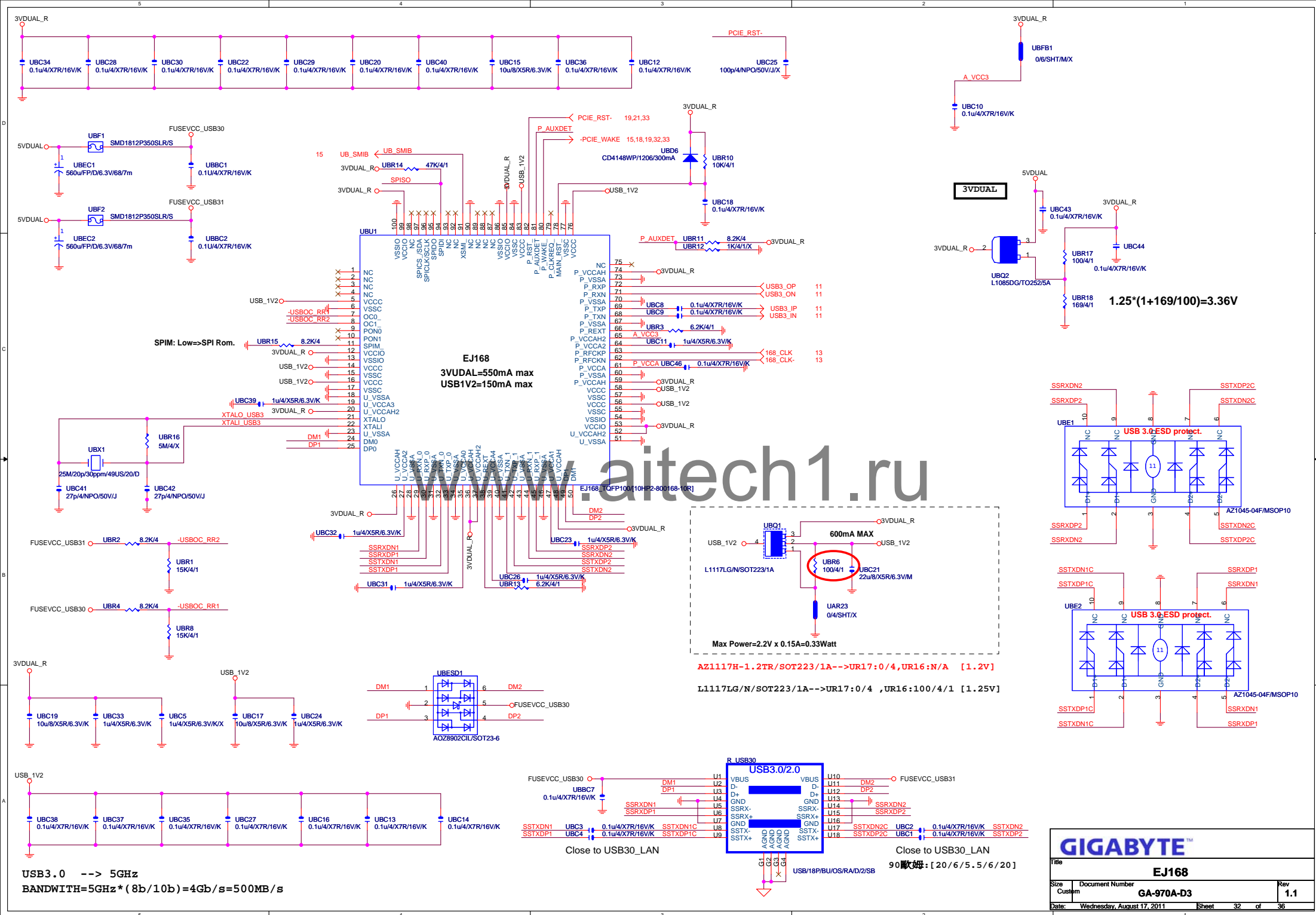
Hardware Monitor circuits











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